TE7009L

PCI-E™ to PCI Bridge

Revision V1.1

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Tenor Electronics Corporation.

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TE7009L

PCI-E™ to PCI Bridge

1. Features

2.1 PCI Express

- PCI Express base rev 1.0a compliant
- PCI Express to PCI bridge rev. 1.0 compliant
- Single one-lane PCI Express connection
- 16-bit CRC on all link message information
- 32-bit CRC covering all transmitted data packets
- Error forwarding supported, including data poisoning and PCI bus parity errors
- PCI Express advanced error reporting capability
- Support up to 512 bytes variable size of read request
- Support up to 512 bytes variable payload size
- Support 100MHz PCI Express differential reference clock
- Secondary side initialization via Type 0 configuration cycles supported

2.2 PCI

- PCI local bus rev. 3.0 compliant
- 32-bit, 33/66 MHz, 3.3V PCI, but no 5V tolerant
- 5 external REQ/GNT pairs for internal arbiter
- PCI LOCK operation supported
- Support up to 2 PCI delayed transaction, including memory read, I/O read/write, and configuration read/write
- Support clock run operation

2.3 Power Management

- PCI Express Active Power Management states (ASPM): L0s and L1
- Link power management: L0, L0s, L1, L2 in-band beacon generation Integrated AUX power plane
- Support PCI Power Management Rev 1.1: D0, D1, D2, D3hot and D3cold device power states
- Support PME event propagation on behalf of PCI devices
- Side-band WAKE# signals

2.4 SMBus

- System Management Bus rev. 2.0
- Only Slave-mode operation supported
- PCI Express PHY is configured via SMBus

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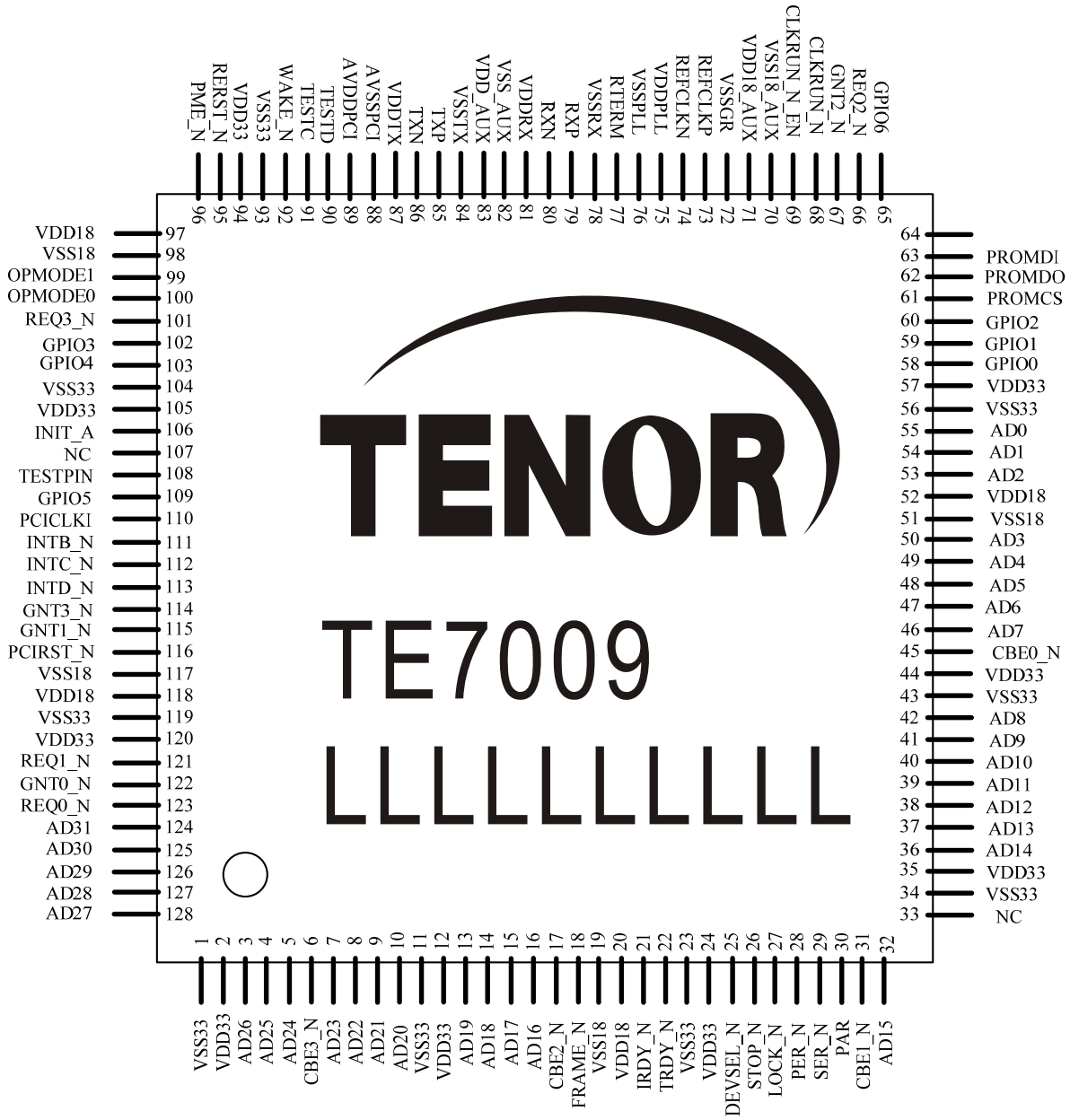
2. Overview

PCI Express is a high-speed interconnection technology which is used to achieve high performance and flexible connections in box at competitive cost. The TE7009 PCI-E to PCI Bridge provides a solution to connect PCI Express with existing PCI devices. It features a PCI Express primary interface and a PCI secondary interface. With connected to a PCI-E to PCI bridge existing PCI devices can be used continuously on a PCI-E card by plug the PCI-E card into a PCI-E slot in a PC.

3. PIN CONFIGURATION



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4. PIN DESCRIPTION

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VSS33	33	NC	65	GPIO6	97	VDD18
2	VDD33	34	VSS33	66	REQ2_N	98	VSS18
3	AD26	35	VDD33	67	GNT2_N	99	OPMODE1
4	AD25	36	AD14	68	CLKRUN_N	100	OPMODE0
5	AD24	37	AD13	69	CLKRUN_N_EN	101	REQ3_N
6	CBE3_N	38	AD12	70	VSS18_AUX	102	GPIO3
7	AD23	39	AD11	71	VDD18_AUX	103	GPIO4
8	AD22	40	AD10	72	VSSGR	104	VSS33
9	AD21	41	AD9	73	REFCLKP	105	VDD33
10	AD20	42	AD8	74	REFCLKN	106	INTA_N
11	VSS33	43	VSS33	75	VDDPLL	107	NC
12	VDD33	44	VDD33	76	VSSPLL	108	TESTPIN
13	AD19	45	CBE0_N	77	RTERM	109	GPIO5
14	AD18	46	AD7	78	VSSRX	110	PCICLKI
15	AD17	47	AD6	79	RXP	111	INTB_N
16	AD16	48	AD5	80	RXN	112	INTC_N
17	CBE2_N	49	AD4	81	VDDRX	113	INTD_N
18	FRAME_N	50	AD3	82	VSS_AUX	114	GNT3_N
19	VSS18	51	VSS18	83	VDD_AUX	115	GNT1_N
20	VDD18	52	VDD18	84	VSSTX	116	PCIRST_N
21	IRDY_N	53	AD2	85	TXP	117	VSS18
22	TRDY_N	54	AD1	86	TXN	118	VDD18
23	VSS33	55	AD0	87	VDDTX	119	VSS33
24	VDD33	56	VSS33	88	VAVSSPCI	120	VDD33
25	DEVSEL_N	57	VDD33	89	AVDDPCI	121	REQ1_N
26	STOP_N	58	GPIO0	90	TESTD	122	GNT0_N
27	LOCK_N	59	GPIO1	91	TESTC	123	REQ0_N
28	PER_N	60	GPIO2	92	WAKE_N	124	AD31
29	SER_N	61	PROMCS	93	VSS33	125	AD30
30	PAR	62	PROMDO	94	VDD33	126	AD29
31	CBE1_N	63	PROMDI	95	RERST_N	127	AD28
32	AD15	64	PROMSK	96	PME_N	128	AD27

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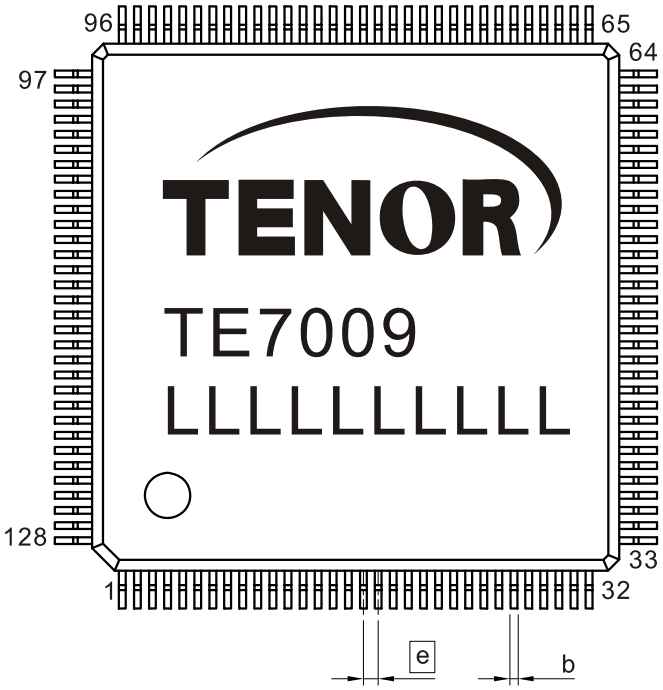
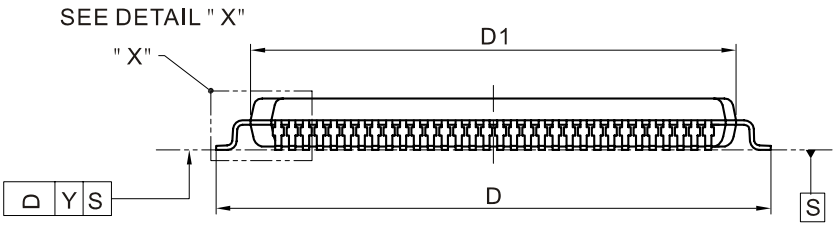
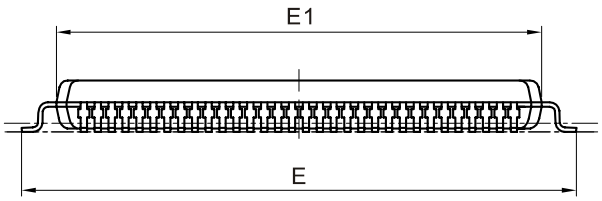
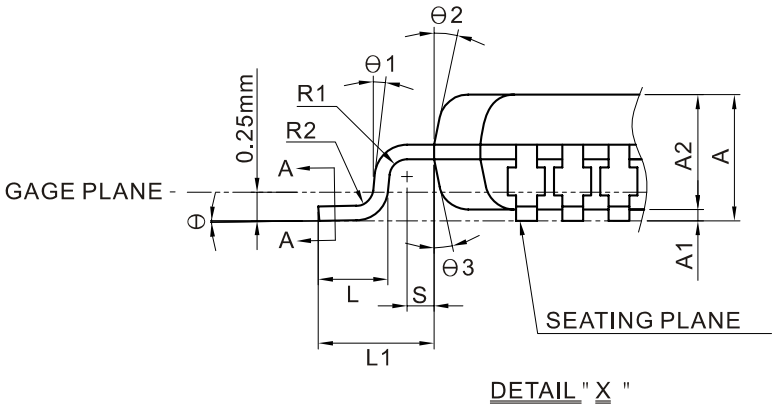
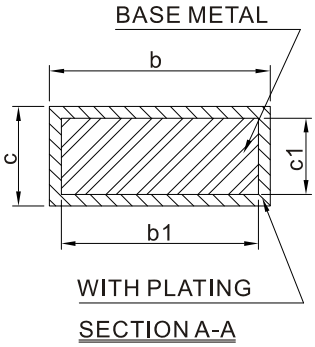
5. Package Dimensions











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SYMBOL	DIMENSION(MM)			DIMENSION(NIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.6			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6.3	7.5
c	0.09		0.2	4		8
c1	0.09		0.16	4		6
D	16.00 BSC			630 BSC		
D1	14.00 BSC			551 BSC		
E	16.00 BSC			630 BSC		
E1	14.00 BSC			551 BSC		
e	0.40 BSC			16 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
s	0.20			8		

Note.

REFER TO JEDEC MS-026 / BBC

DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.

DIMENSION b DOES NOT INCLUDE DAMBER PRODTUSION. ALLOWABLE THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

ALL DIMENSIONS IN MILLIMETERS.

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